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TECHNICAL REPORT

# Design Science for Radiation-effects Rate Prediction and Development of Error-immune Circuitry



November 2018

HDTRA1-10-1-0013

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Prepared by:
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**14. ABSTRACT**

The overall goal of this project at Brown University in collaboration with Vanderbilt University and MIT-Lincoln Labs was to create a validated methodology for predicting single-event error rates and to design complex radiation-tolerant integrated circuits. The project followed three fundamental thrusts: 1) development of a statistical technique to predict the radiation-induced and thermal fluctuation-induced single-event upset (SEU) rate; 2) development of an error-immune circuit design style; and 3) validation of the design methodology and the statistical error-prediction technique using a fully-depleted (FD) SOI CMOS fabrication technology.

**15. SUBJECT TERMS**

Error-rate modeling; noise analysis; noise-immune circuit design; logic synthesis; ultimate CMOS

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## U.S. customary units to and from international units of measurement*

| U.S. Customary Units | Multiply by → / ← Divide by† | | International Units |
|---|---|---|---|
| **Length/Area/Volume** | | | |
| inch (in) | 2.54 | $\times 10^{-2}$ | meter (m) |
| foot (ft) | 3.048 | $\times 10^{-1}$ | meter (m) |
| yard (yd) | 9.144 | $\times 10^{-1}$ | meter (m) |
| mile (mi, international) | 1.609 344 | $\times 10^{3}$ | meter (m) |
| mile (nmi, nautical, U.S.) | 1.852 | $\times 10^{3}$ | meter (m) |
| barn (b) | 1 | $\times 10^{-28}$ | square meter ($m^2$) |
| gallon (gal, U.S. liquid) | 3.785 412 | $\times 10^{-3}$ | cubic meter ($m^3$) |
| cubic foot ($ft^3$) | 2.831 685 | $\times 10^{-2}$ | cubic meter ($m^3$) |
| **Mass/Density** | | | |
| pound (lb) | 4.535 924 | $\times 10^{-1}$ | kilogram (kg) |
| unified atomic mass unit (amu) | 1.660 539 | $\times 10^{-27}$ | kilogram (kg) |
| pound-mass per cubic foot (lb $ft^{-3}$) | 1.601 846 | $\times 10^{1}$ | kilogram per cubic meter (kg $m^{-3}$) |
| pound-force (lbf avoirdupois) | 4.448 222 | | newton (N) |
| **Energy/Work/Power** | | | |
| electron volt (eV) | 1.602 177 | $\times 10^{-19}$ | joule (J) |
| erg | 1 | $\times 10^{-7}$ | joule (J) |
| kiloton (kt) (TNT equivalent) | 4.184 | $\times 10^{12}$ | joule (J) |
| British thermal unit (Btu) (thermochemical) | 1.054 350 | $\times 10^{3}$ | joule (J) |
| foot-pound-force (ft lbf) | 1.355 818 | | joule (J) |
| calorie (cal) (thermochemical) | 4.184 | | joule (J) |
| **Pressure** | | | |
| atmosphere (atm) | 1.013 250 | $\times 10^{5}$ | pascal (Pa) |
| pound force per square inch (psi) | 6.984 757 | $\times 10^{3}$ | pascal (Pa) |
| **Temperature** | | | |
| degree Fahrenheit ($^oF$) | $[T(^oF) - 32]/1.8$ | | degree Celsius ($^oC$) |
| degree Fahrenheit ($^oF$) | $[T(^oF) + 459.67]/1.8$ | | kelvin (K) |
| **Radiation** | | | |
| curie (Ci) [activity of radionuclides] | 3.7 | $\times 10^{10}$ | per second ($s^{-1}$) [becquerel (Bq)] |
| roentgen (R) [air exposure] | 2.579 760 | $\times 10^{-4}$ | coulomb per kilogram (C $kg^{-1}$) |
| rad [absorbed dose] | 1 | $\times 10^{-2}$ | joule per kilogram (J $kg^{-1}$) [gray (Gy)] |
| rem [equivalent and effective dose] | 1 | $\times 10^{-2}$ | joule per kilogram (J $kg^{-1}$) [sievert (Sv)] |

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†Multiply the U.S. customary unit by the factor to get the international unit. Divide the international unit by the factor to get the U.S. customary unit.

# Final Report

# Design Science for Radiation-effects Rate Prediction and Development of Error-immune Circuitry

## Award Number: HDTRA1-10-1-0013

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June 30, 2015

## 1. Project Summary

The overall goal of grant HDTRA1-10-1-0013 at Brown University in collaboration with Vanderbilt University and MIT–Lincoln Labs was to create a validated methodology for predicting single-event error rates and to design complex noise-tolerant integrated circuits. The project followed three fundamental thrusts:

A. The development of a statistical technique to predict the radiation-induced and thermal fluctuation-induced single-event upset (SEU) rate at the device and sub-circuit level that builds on Monte Carlo simulations of radiation energy deposition but goes beyond Monte Carlo circuit response simulations to provide a numerically tractable solution of rare events.

B. The development of an error-immune circuit design style based on our probabilistic computing paradigm. In particular, our design style assumes that not all logic signals are reliable at any given time, but the overall computation result must meet the required reliability specifications in the presence of noise and SEU-inducing radiation. This design methodology was to be implemented using standard CMOS gates to meet a specified reliability-performance benchmark.

C. The validation of the design methodology and the statistical error-prediction technique using a fully-depleted (FD) SOI CMOS fabrication technology optimized for low-voltage operation, as well as possibly advanced bulk CMOS technology.

Significant contributions were made on all three research thrusts, as detailed below.

### *Thrust 1: Error Prediction Modeling*

The statistical technique development for predicting thermal-noise and radiation-induced SEU rates was successfully completed. This effort was spearheaded by a DTRA-supported Brown graduate student (P. Jannaty), in close collaboration with the Vanderbilt group on the radiation-induced errors. We obtained two numerical solutions: a full matrix Markov-chain based solution for noise in subthreshold devices subject to thermal noise and alpha particle upsets, and an extension of the approach to above-threshold ultimate CMOS. This project formed the core of P. Jannaty's PhD thesis on this topic (granted in May, 2012), and led to the following publications:

[1] P. Jannaty *et al.*, "Numerical queue solution of thermal noise-induced soft errors in subthreshold CMOS devices", *Proc. ACM GLSVLSI* (2010), pp. 281-286.

[2] P. Jannaty *et al.*, "Two-dimensional Markov chain analysis of radiation-induced soft errors in subthreshold nanoscale CMOS devices", *IEEE Trans. Nucl. Sci.* **57**, 3768 (2010).

[3] P. Jannaty *et al.*, "Full two-dimensional Markov chain analysis of thermal soft errors in subthreshold nanoscale CMOS devices", *IEEE Trans. Dev. Mater. Reliability* **11**, 50 (2011).

[4] P. Jannaty *et al.*, "Shot noise-induced failure in nanoscale flip-flops. Part I: Numerical framework", *IEEE Trans. Electron Dev.* **59**, 800 (2012).

[5] P. Jannaty *et al.*, "Shot noise-induced failure in nanoscale flip-flops. Part II: Failure rates in 10-nm ultimate CMOS", *IEEE Trans. Electron Dev.* **59**, 807 (2012).

Finally, the last few months of this project was spent developing a simulation framework for analyzing transient effects due to thermal noise in sub-threshold circuits, work spearheaded by another DTRA-supported graduate student at Brown, M. Donato and led to the following publication:

[6] Marco Donato *et al.*, "A Simulation Framework for Analyzing Transient Effects Due to Thermal Noise in Sub-Threshold Circuits," *ACM Great Lakes Symposium on VLSI Design (GLSVLSI),* pp. 45-50. (May 2015).

Numerical modeling of thermal noise in subthreshold devices was first highlighted in [1],[3]. In particular, we found a complete numerical solution for a full 2D Markov queue with Poissonian statistics, solving the thermal noise fluctuations in a flip-flop inverter operated in the subthreshold regime. We also completed work on numerical modeling of alpha-particle induced upsets in subthreshold devices [2]. In this work, an analytical framework based on 2D Markov queue theory combined with MRED charge deposition simulations solved alpha particle-induced soft-error rates of a flip-flop operated in the subthreshold regime.

Later work spearheaded by P. Jannaty focused on above-threshold modeling of noise in advanced devices [4],[5]. The 2D Markov queue approach was successfully extended to above-threshold devices by incorporating the non-Poissonian statistics of electron transfer between queue states of a flip-flop in an end-of-roadmap 10-nm gate length CMOS technology. The current and noise characteristics of individual double-gate transistors were calculated using non-equilibrium Green's function (NEGF) formalism. Of the two papers published in *IEEE Trans. Electron Devices*, the first one focuses on laying out the general formalism [4], and the other on presenting simulated time-to-failure results [5].

As mentioned earlier, the last few months of this project was spent developing a simulation framework for analyzing transient effects due to thermal noise in sub-threshold circuits [6]. When considering thermal noise, a correct modeling approach has to go beyond the additive white Gaussian noise used in classical noise analysis. Monte Carlo simulations can be used to expose rare soft errors, but are computationally prohibitive and the probabilistic approaches we developed during the earlier part of this project do not provide any insight about the dynamic response to noise events. In this latest work, we developed a time-domain model for fundamental technology-independent thermal noise in sub-threshold circuits. Among other things, this model can be used to generate noise input files for SPICE transient analysis, which will be extremely important for our noise-immune circuit design effort.

Our model in [6] requires an understanding of how the statistics of the Poissonian processes describing the charging and discharging rates are affected by the time-varying physical characteristics of the devices. It also requires techniques that allow for simulations over relatively long time frames to capture rare errors that cannot be seen in standard Monte Carlo simulations. We used the Onstein-Uhleneck process to capture

correct dynamic responses and have guaranteed correct model behavior to varying biasing conditions using non-homogeneous Poisson processes. Our model can noticeably decrease the simulation time of long thermal noise time–series allowing us to capture rare events not only significantly faster than conventional SPICE simulations (i.e., with a 47X speedup), but also with comparable physical accuracy, as shown in Fig. 1 below.

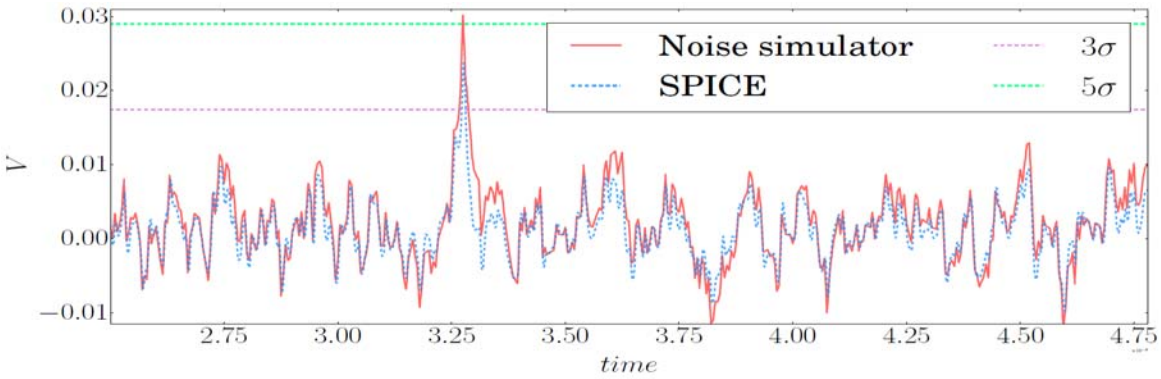


**FIG. 1. Comparison of the time series generated by our simulator and the SPICE transient response to the shot-noise currents. Thresholds for the noise events were set at 3σ and 5σ, where σ = $(kT/C)^{1/2}$.**

## *Thrust 2: Error-Immune Circuit Design*

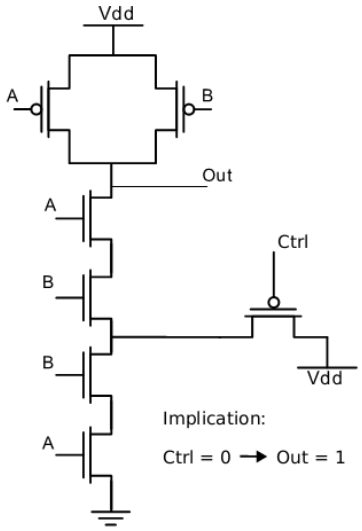


**FIG. 2. A modified Schmitt NAND gate used for implication reinforcement. Note that the control signal (labeled *Ctrl*) comes from another node in the circuit and is used to help keep the value of the output at logic 1 when the control signal *Ctrl* has a logic value of zero.**

The error-immune design style work, also led by M. Donato, with help from Brown visitors and undergraduate students, has led to the development of a new noise-immune differential Schmitt-trigger logic style (see Fig. 2) and its extension to larger logic circuits using selective reinforcement of key nodes to avoid excessive area overhead. This new design paradigm has been published and presented as follows:

[7] M. Donato *et al.*, "Designing noise-immune CMOS circuits for sub-threshold operation using Schmitt-trigger logic", *IEEE North Atlantic Test Symposium* (May, 2011), *best student presentation award.*

[8] Warren Jin, "A Schmitt-Trigger-Based Approach to Noise-Immune Sub-Threshold Circuit Design," *ScB Honors Thesis*, Brown University, (May 2012)

[9] M. Donato *et al.*, "A noise-immune subthreshold circuit design based on selective use of Schmitt-trigger logic", *Proc. ACM Great Lakes Symp. VLSI* (2012), pp. 39-44.

[10] Lauren Moser, "Modeling optimal Schmitt trigger based implication chains for noise-immune sub-threshold circuits," *ScB Honors Thesis*, Brown University, (May 2013).

[11] A. Mazumdar *et al.*, "An automated synthesis tool for generating noise-immune sub-threshold Circuits," *2013 Brown Summer Research Symp.*, (August 2013)

[12] M. Donato *et al.*, "A synthesis tool for designing noise-immune circuits via selectively-reinforced logic," *IEEE Workshop on Silicon Errors in Logic – System Effects (SELSE)*, (April 2014).

We were able to get the framework of the automated synthesis tool in place, which allows us to analyze larger logic circuits and select the optimum number and location of nodes that can be reinforced given an allowed area overhead. The project ended with additional work (in preparation for publication) on minimizing the number of Schmitt-trigger reinforcement. Validating this approach in simulation, including an analysis of noise tolerance *vs.* area overhead *vs.* power-performance trade-off requires extensive circuit simulation, and was part of our latest efforts during the final year of the project [6].

Using our differential Schmitt-trigger logic gates, we developed a procedure for reinforcing only certain logic nodes along a selected path, from primary inputs to primary outputs [7],[8],[9]. The reinforcement reflects a logic implication that already exists between two nodes in the circuit (see Fig. 3). This was our starting point for further evaluating the noise sensitivity of a circuit to the placement of Schmitt-trigger gates and the logic implications they are reinforcing. From these evaluation results, we have developed the framework of our synthesis tool that allows us to analyze a logic circuit and automatically choose which logic implications to reinforce using our Schmitt-trigger gates [10].

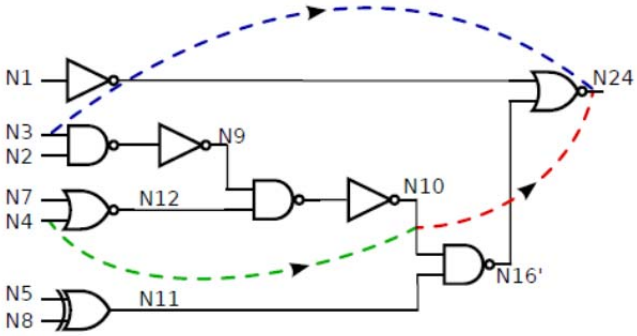


**FIG. 3. Example circuit show 3 existing logic implications, N3=0→N24=0, N4=1→N10=0, N10=0→N24=0.**

We have found that exactly which nodes are targeted for selective reinforcement using our Schmitt-trigger gates can have a significant impact on the noise immunity of the circuit [11], [12]. Targeting nodes that have a high likelihood of generating an observable fault at a primary output may be particularly worthwhile. Signal value probabilities also play a significant role in choosing the best implication to reinforce with the Schmitt-trigger gate. These observations will play a key role in further development of our automatic synthesis tool.

The project ended with additional (but yet-to-be-published) work on minimizing the number of Schmitt-trigger reinforcement such that optimal noise-immunity can be achieved within an allowed area overhead. Validating this approach in simulation, including an analysis of noise tolerance *vs.* area overhead *vs.* power-performance trade-off requires extensive circuit simulation, and was part of our latest efforts during the final year of the project. As such, a key element to successfully accomplishing this task in the future will be development of the tool for analyzing transient effects due to thermal noise. Initial work on this front was published in [6], with ongoing efforts even after the grant ended in September 2014.

## *Thrust 3: Experimental Validation*

The experimental validation of the error rate predictive machinery and the noise-immune logic designs required the fabrication of two types of test circuits: large arrays of flip-flops to monitor thermal- or radiation-induced error rates, and different variants of noise-immune test circuits together with standard CMOS designs for comparison. The first Brown-designed FD-SOI test site, containing ultralow $V_{DD}$ transistors at 150 nm gate length, was fabricated by MIT-Lincoln Labs and delivered in 2011. This design included a bank of 100 flip-flops to test error rates in thermal and radiation environments, as well as small noise-immune test circuits. Initial results were reported in the following:

[13] M. Donato *et al.*, "Designing, fabricating, and testing noise immune circuits", *2011 Subthreshold Microelectronics Conference* (Sept. 2011, Lexington, MA).

[14] M. P. King *et al.*, "Electron-induced single-event upsets in static random access memory," *IEEE Trans. on Nuclear Sci.* vol. 60, no. 6, pp. 4122-4129 (Dec. 2013)

[15] M. P. King *et al.*, "Electron-induced single-event upsets in static random access memory," *IEEE Nuclear Space Radiation Effects Conf.* (*NSREC–2013*), (July 2013).

Since the initial testing, a custom test board was designed and built at Brown and measurements were taken both at Brown (thermal environments up to $T = 80\ ^{o}C$) and at Vanderbilt (radiation environment using a Sr-90 source). The devices and flip-flops were tested by DTRA-supported Brown graduate students (X. Hou and M. Donato) for correct operation at low $V_{DD}$ down to 90 mV with current drive and stability tuned via the backgate voltage $V_{BG}$, as shown in Fig. 4.

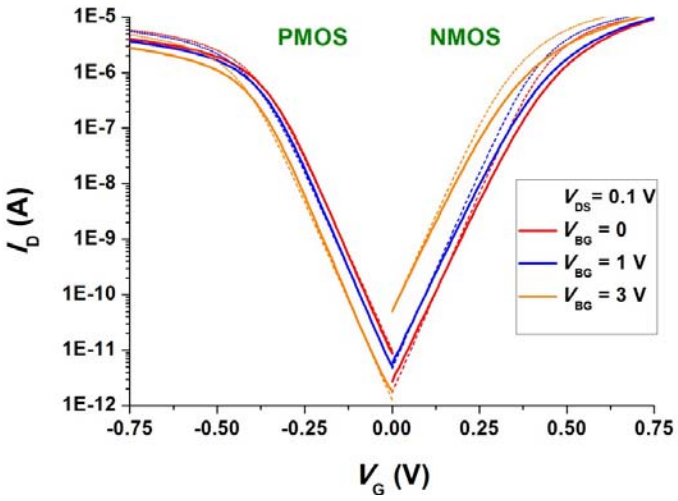


**FIG. 4. Drain currents of both NMOS and PMOS as a function of front gate voltage, $V_G$, under different $V_{BG}$ at fixed $V_{DD}$ = 0.1 V and $T$ = 25 °C. It is clearly shown that they are perfectly matched at $V_{BG}$ = 1V (blue lines).**

The thermal error rates in flip-flop banks were measured at Brown as a function of $T$, $V_{DD}$ and $V_{BG}$ while the radiation upset measurements were completed at Vanderbilt (with help of partially DTRA-supported Vanderbilt graduate students Michael King and Stephanie Weeden-Wright). The thermal upset rates in flip-flop banks intentionally detuned from maximum stability via $V_{BG}$ were found to follow Poissonian statistics.

Our measurements of thermal upset rates in flip-flop banks as a function of $V_{DD}$, $T$ and $V_{BG}$ are shown in Fig. 5. Figure 5(a) shows the stability diagram, expressed as the noise margin *vs.* $V_{BG}$-tuned current mismatch between NMOS and PMOS transistors in the flip-flop at $T$ = 25 °C for various ultra-low supply voltages $V_{DD}$ = 90–140 mV. The states below the 22 mV noise margin (red dots) are unstable. The corresponding measured error rates for $V_{DD}$ = 110 mV and $T$ = 25, 60 and 80 °C are shown in Fig. 5(b), with the 66,000 errors/hour maximum error rate due to the finite sampling speed of the custom-designed measurement board. We observed the expected activated behavior of the error rate with $T$ and with the current mismatch: at higher $T$, the thermal noise is higher, leading to higher error rates at the same current mismatch, so the stable region shifts towards $V_{BG}$ = 1 V, where the NMOS and PMOS transistors are matched (see Fig. 4).

The error distribution of each individual measurement can be statistically plotted as a function of time to error. In Fig. 6, error distributions of two different $V_{BG}$ are plotted at $V_{DD}$ = 110 mV and $T$ = 80 °C. The Poissonian nature of the time-to-error distribution confirms the existence of uncorrelated thermal noise source, which is a significant result that validates the theoretical framework. Mean time-to-error is shortened by one order of magnitude at $V_{BG}$ = 1.75 V (0.137 s) compared to 1.72 V (1.032 s), indicating the sensitivity of the error rate to NMOS-PMOS mismatch. The dependence of the mean time-to-error on the $V_T$ mismatch is consistent with the statistical modeling and with the TCAD modeling of the noise margin, shown in the inset of Fig. 6.

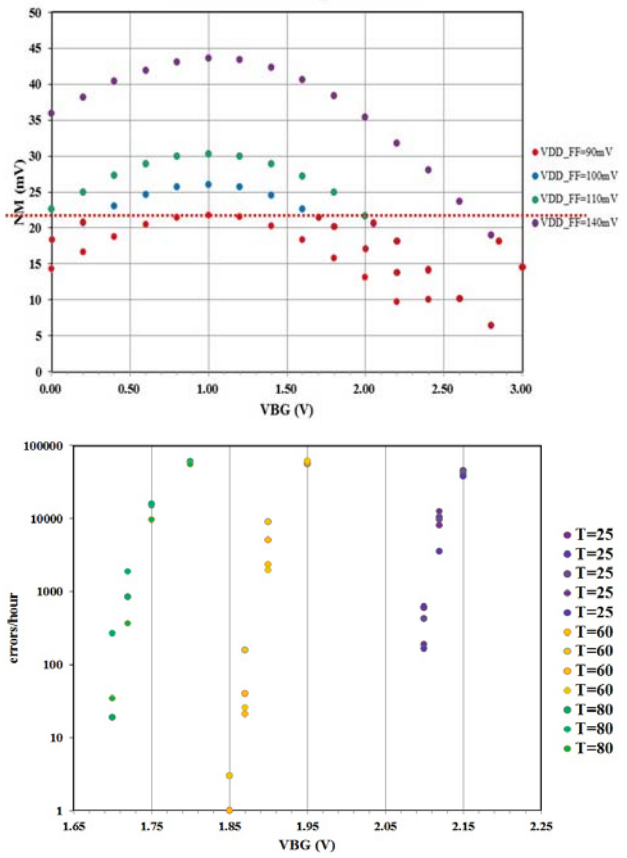


**FIG. 5. (a) Noise margin *vs.* $V_{BG}$ at $T$ = 25 °C under $V_{DD}$ = 90, 100, 110, and 140 mV. Red dots indicate thermally unstable points where errors are experimentally detected, defining a noise margin of ~22 mV; (b) Error rate (per hour) *vs.* $V_{BG}$ at $V_{DD}$ = 110 mV under $T$=25, 60, and 80 °C. As $T$ increases from 25 °C , the error boundary moves from to $V_{BG}$ = 2.05 to 1.8 and to 1.65 V, closer to $V_{BG}$ = 1 V point of matched NMOS-PMOS currents.**

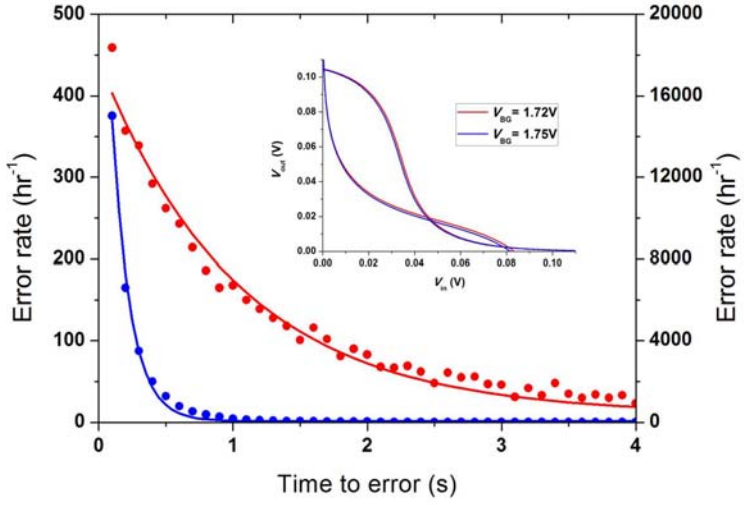


**FIG. 6. Thermally induced error rate as a function of time-to-error with $V_{DD}$ = 110 mV and $T$ = 80 °C, under two different $V_{BG}$ = 1.72 and 1.75 V. Data points (solid dots) are fit by Poisson distribution (solid lines). Inset shows both transfer characteristics and noise margin of the flip-flop, simulated by Sentaurus TCAD, calibrated from experimental transistor data.**

A difficulty with statistical validation of noise-immune logic designs for longer time-to-error regimes arose because of the limited number of flip-flops in the original test flip-flop bank. An improved FD-SOI design, including an updated flip-flop bank (increasing the number of flip-flops from 100 to 10,000), corrections in test circuitry for our noise-immune logic designs, and new Schmitt-trigger logic noise-immune circuits was ported to the next generation of the MIT-LL ultralow $V_{DD}$ technology at $L_G$ = 90 nm design rule. However, due to various delays, we did not receive the chips until after completion of the grant. Nevertheless, we hope to test these chips and validate our designs at a future date using alternative funding sources. Similarly, in collaboration with Vanderbilt, we ported the Schmitt-trigger designs to an advanced foundry bulk CMOS process at the $L_G$ = 40 nm node. While a fabrication run in bulk CMOS was not included in this project, we hope to use this in future extensions of the project.

The second validation thrust was to validate the radiation-induced error rates in our flip-flop banks, in collaboration with the Vanderbilt team (particularly the DTRA-supported Vanderbilt graduate student S. Wheedon-Wright). Two radiation measurement visits were undertaken to test the error statistics in the presence of alpha particle radiation as a function of alpha flux (400 or 700 particles/mm$^2$s), $V_{DD}$, and $V_{BG}$. A typical example of the error statistics at $V_{DD}$ = 300 mV, $V_{BG}$ = 1 V (matched NMOS-PMOS current drive) is shown in Fig. 7.

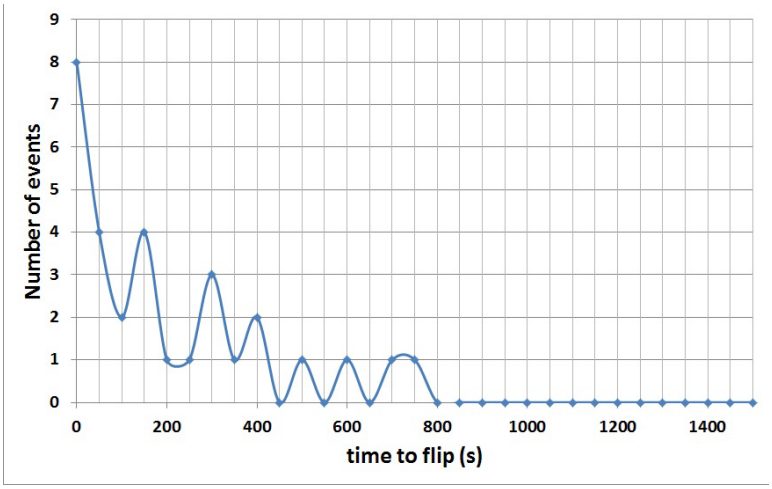


**FIG. 7. Time to error statistics on a flip-flop test bank at $V_{DD}$ = 300 mV, $V_{BG}$ = 1 V, $T$ = 25 °C in an alpha particle flux of 400 particles/mm$^2$s.**

The distribution of time-to-error is consistent with Poissonian statistics, but unlike thermal error data, the confidence is limited by the small number of events, since our circuits would also undergo standard radiation-induced changes in transistor characteristics (due to trapped oxide charge) of become unusable after ~ 10 hours of measurement. We found that error rates would increase as $V_{DD}$ decreased, whereas current mismatch between NMOS and PMOS transistors (set by $V_{BG}$) had little effect. After analysis of the hit rate by the alpha particles, which we had previously estimated

would deposit ~1000 electrons in the active area of an FD-SOI transistor at $L_G$ = 150 nm, we concluded that the upset rate was indistinguishable from the hit rate – every alpha particle event would result in an upset. Measurements on smaller transistors (in which charge deposition would be reduced at least as $L_G^2$, permitting longer measurements and better statistics) are needed for true comparison with theory [2]. We plan a radiation measurement experiment at Vanderbilt in the coming year, once we characterize the $L_G$ = 90 nm FD-SOI lot recently delivered by MIT-LL.

Finally, the Vanderbilt team investigated the sensitivity of 28 nm and 45 nm bulk CMOS SRAMs to radiation from energetic electrons. Experimental results show an exponential dependence on applied bias, with upsets occurring only under reduced bias conditions.

## 4. Supported and Associated Personnel:

*Brown University*

Faculty: R. Iris Bahar, J. Mundy, W. R. Patterson, A. Zaslavsky

Graduate students: DTRA-supported graduate students, Pooya Jannaty, F. Cosmin Sabou, Marco Donato and Xiaoxiao Hou, with Pooya and Cosmin focused on statistical modeling, Marco on circuit design and modeling, and Xiaoxiao on experimental measurements. Visiting student Fabio Cremona also made contributions to the project, but was not supported by this award.

Undergraduate students: Brown computer engineering seniors, Warren Jin and Lauren Moser, worked on their honors theses on logic-implication selection in Schmitt-trigger reinforced circuits; additional support came from Amrita Mazumdar, who spent the summer months from June-August 2013 on the noise-immune synthesis tool.

*Vanderbilt University*

Faculty: R. D. Schrimpf, R. A. Reed, R. A. Weller, M. L. Alles, B. L. Bhuva

Graduate students: Michael King (DTRA-supported until PhD defense), Stephanie Weeden-Wright (during the option year).

*MIT-Lincoln Laboratory*

Staff: P. Gouker, C. Keast, M. Renzi, J. Kedzierski participated in the FD-SOI low-$V_{DD}$ circuit fabrication and furnished two FD-SOI fabrication runs, including a lot of the new $L_G$ = 90 nm FD-SOI devices delivered in spring of 2015 (during the no-cost extension of the option year and currently under characterization).

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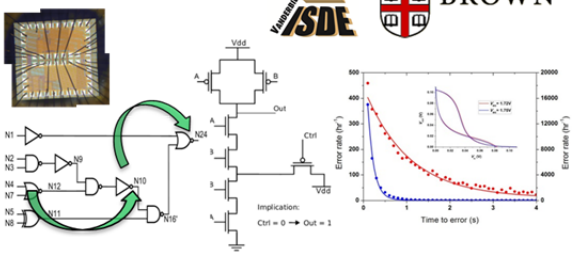
## Design Science for Radiation-effects Rate Prediction and Development of Error-immune Circuitry

PI: R. I. Bahar, Brown University; Co-PIs: A. Zaslavsky, J. Mundy, W. R. Patterson, Brown University;
R. D. Schrimpf, R. A. Reed, R. A. Weller, M. L. Alles, B. Bhuva, Vanderbilt University

Award Number: HDTRA 1-10-1-0013

**Objective:** To create a validated methodology for predicting single-event effect rates and designing noise-immune radiation-tolerant integrated circuits.

**Method:** This proposal addresses the basic scientific advances needed to design radiation immune circuits with end-of-roadmap technology (CMOS-based and beyond).




**Approach:** We developed a ***statistical approach*** to calculate the time-to-failure of future CMOS-based circuits due to radiation-induced events We also developed a fast simulation framework for analyzing transient effects due to thermal noise. We coupled this modeling work with development of ***noise-tolerant circuit design*** approaches and ***fabrication*** in CMOS test circuits using advanced bulk CMOS and FD-SOI processes and ***experimental validation*** through testing of thermally-induced and radiation-induced error rates.

**Personnel Supported:** 9 faculty, 7 graduate and 3 under-grad students supported/associated with this project to date.

**Past Year Publications & Reports:** 2 PhD theses, 2 ScB honors theses, 10 journal/conference papers, 3 workshop presentations.

**Main Tasks:**

- Statistical numerical modeling of error rates in both subthreshold and above-threshold ultimate CMOS
- Design of noise-immune circuits based on Schmitt-trigger gates that reinforce correct logic implications
- Testing of both thermally- and radiation-induced error rates in test circuits, with comparison to statistical theory
- Fabrication of noise-immune circuits in advanced CMOS processes followed by characterization/validation

**Funding period:** 3/15/2010-9/30/2014
$1.05M (3 years) + $350K (option year + no cost extension)

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